REMARKS

This Reply is being filed in response to the Final Office Action dated February 1, 2010.

Claims 1, 3-14 and 16-25 are pending in this application. In the Office Action, independent claim 1 was rejected as being obvious over US 2003/0046324 to Sukuki et al. ("Suzuki"), US 2002/0152185 to Jamadagni ("Jamadagni"), 4,538,235 to Henning ("Henning") and 5,748,967 to Nakamura et al. ("Nakamura"). Independent claim 13 was rejected as being obvious over Suzuki, Jamadagni, Henning, Nakamura and US 2003/0197632 to Rubin et al. ("Rubin").

These rejections are traversed on the grounds that the differences between the claimed subject matter as a whole and the cited references are such that the present claims would not have been obvious to one of ordinary skill in the art.

The newly-cited Nakamura reference is related to systems and methods of rewriting PROMs in microprocessors, and is not relevant to real-time event management methods and systems as presently claimed.

Nakamura was cited for disclosing a "first memory" and a "second memory." However, Nakamura actually discloses a multiprocessor system having two independent systems, each with a microprocessor (2a, 2b), a memory (3a, 3b) and a data bus (101, 102).

By contrast, the event management method and system of the present invention recites an independent management unit with one

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data bus and two memories ("first memory," "second memory"). The first memory stores events to be processed in real time by the independent management module and the second memory stores events so that they can be read by the data bus.

The present invention is distinguishable from Nakamura at least on the grounds that in Nakamura there are two microprocessors and two memories, in contrast with the present invention in which there is one microprocessor and one data bus with two memories. Nakamura teaches that each memory (3a, 3b) is connected to an associated bus (101, 102). It is an essential feature of Nakamura that both memories (3a, 3b) exchange data with the data bus, since in order to rewrite a program in memory 3a "rewrite data is transferred via the bus 101 thereto under control of processor 2a," and in order to rewrite a program in memory 3b "rewrite data is transferred thereto via the bus 102 under control of the processor 2a." (See col. 3, lines 33-38).

Furthermore, the memories (3a, 3b) of Nakamura are Programmable Read-Only Memories (PROMs) that store *executable programs* for use with their associated microprocessors (2a, 2b). They do not store received events to be processed in real-time by an independent management unit, as presently claimed. By contrast, Nakamura teaches a relatively complex scheme for rewriting data in the PROMs that involves the host computer 1, a plurality of intermediate circuit elements 5, 6, 7, and 8, and a process in which a microprocessor from a first independent system temporarily takes control of the bus and PROM associated with the second independent system in order to write data to the PROM of the second independent system. (See col. 3, line 15 through col.

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4, line 65). This is entirely inconsistent with the real-time event management methods and systems of the present invention, and it does not even appear possible that the system of Nakamura could be used for real-time event management as presently recited.

Therefore, Nakamura is clearly distinguishable from the method and system of claims 1 and 13, respectively.

Applicant further asserts that the Examiner has not provided sufficient explanation and reasoning to support the final rejections for obviousness under § 103. The present rejections appear to be simply a piling on of selective features of disparate references without regard to how they might suggest being combined, or whether they are even combinable. It is the Examiner's burden to provide some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. The Examiner has not provided any rational basis for combining the features of these numerous references to provide the event management method and system of the present claims.

For example, the Examiner has not shown why one of ordinary skill in the art would combine the primary Suzuki reference, which relates to managing the execution order of a plurality of tasks in a programmable logic controller based on the classification of the tasks (i.e., communication task group, control task group, management task group), with the Jamadagni reference, which is directed to the very different problem of correlating events in order to detect faults in a network system.

Also, as discussed in the previous Amendment, Henning's "interval counter circuitry" lacks numerous features of the

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present event management method and system, such the independent management module that time-stamps received events, stores the received events in first and second memories, and assigns at least one appropriate action to each received event. These differences are not addressed in the Final Office Action. Further, the Examiner's stated rationale for combining Henning with Suzuki and Jamadagni ("to allow computer processor control over the detection of external events, prior interval counter circuitry has been inadequate to provide the needed performance") is overbroad, conjectural, and unclear.

The combination of Nakamura is similarly deficient. As stated above, Nakamura relates to a multiprocessor having two independent systems, and describes a scheme by which one microprocessor from one independent system can temporarily take control over, and write to, a memory associated with a second independent system. No rational basis is provided for how or why one would incorporate the two memories described Nakamura into the very different systems described in the Suzuki, Jamadagni and Henning references. The stated explanation that "this guarantees reliability of operation of the microprocessor, the number of ROM change operations is disadvantageously limited," is again overbroad and nonsensical.

Finally, as the applicants have repeatedly pointed out in previous Amendments, the primary Suzuki reference strongly teaches away from the present independent management module that operates in real-time without intervention by the central unit. Suzuki teaches precisely the opposite of this feature, explicitly stressing that all of the processing is performed by a single,

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central unit (CPU). (See para. [0081]). This teaching away by the primary reference evidences the non-obviousness of the present invention. However, the Examiner has not yet addressed the issue of Suzuki's teaching away from the present invention.

In view of the above, it is believed that all rejections are overcome, and that the present application is allowable. Reconsideration is requested.

The Examiner is encouraged to telephone the undersigned attorney to discuss any matter which would expedite allowance of the present application.

Respectfully submitted,

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